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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,105	12/30/2005	Misao Takakusaki	1592-0159PUS1	4561

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EXAMINER	
SONG, MATTHEW J	
ART UNIT	PAPER NUMBER
1714	

NOTIFICATION DATE	DELIVERY MODE
10/12/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/563,105	TAKAKUSAKI ET AL.	
	Examiner	Art Unit	
	MATTHEW SONG	1714	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-3 and 5* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-3 and 5* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/30/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/23/2010 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokogawa et al (US 2003/0141518) in view of Kashima et al (JP 07-086162), an English Abstract and Computer Translation (CT) are provided.

Yokogawa et al teaches a High electron mobility transistor structure including a heterojunction comprising an InP substrate, an InAlAs layer **502**, an InGaAs layer **503**, an n-InAlAs layer **504** and an InP layer **505** serving as an etch stopping layer (para [0003], [0008] and [0048]). Yokogawa et al also teaches using MBE (para [0103]) and using source material beams of In, Al, and As to form InAlAs (para [0154]), which clearly suggests a first step of irradiating beams of at least one group III element and a molecular beam of a first group V element to form a first compound semiconductor layer. Yokogawa et al also teaches forming an InP layer epitaxial as an etching stopping layer (para [0160]), which clearly suggests supplying source beams of a group III element (In) and a group V element (P).

Yokogawa et al does not teach a second step of stopping the irradiation of the molecular beam of the group III element and the molecular beam of the first group V element and halting growth for period of time until a remaining molecular beam intensity of the first group V element is reduced to be in the range of 0.01 to 0.1 of that in the first step.

In a method of forming a heterostructure film, Kashima et al teaches supplying a group IIIa and Va material to grow a IIIaVa thin film using gas source molecular beam epitaxy (Abstract, Fig 1, and CT [0005]-[0007]), which clearly suggests a first step of irradiating a molecular beam of at least one group III element and a molecular beam of a first group V element to form a first compound semiconductor layer. Kashima et al also discloses supply to a substrate of a Va group material is suspended and t2 time discontinuation of the supply of all thin

film raw materials to a substrate is carried out to terminate growth of the IIIaVa thin film (Abstract, Fig 1 and CT [0005]), this clearly suggests a second step of stopping the irradiation of the molecular beam of the group III element and the molecular beam of the first group V element because Kashima et al teaches a time period t2 where all raw materials are suspended (CT [0002]). Kashima et al also teaches supplying a Vb and IIIb material to grow a IIIbVb thin film after the time period t2. (Abstract and [0005]). Kashima et al also teaches forming a heterostructure of InGaAs and InP (CT [0007] and Fig 2, 4 and 5). Kashima et al also teaches source gases of As are efficiently exhausted in the growth vessel and filled up with the gas containing P (CT [0007]).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Yokogawa et al by stopping the flow of reactants for a sufficient period of time, as taught by Kashima et al, between layers of a heterojunction to control the deposition of superfluous group V or Group III elements in the heterointerface, thereby forming a steep heterointerface (CT [0006]).

The combination of Yokogawa et al and Kashima et al does not explicitly teach halting growth for a period of time until the remaining molecular beam intensity of the first group V element is reduced to a range of 0.01 to 0.1 of that in the first step. Kashima et al teaches by adjusting supply downtime t_2, deposition of superfluous group Va element in a heterointerface is controlled and it is very steep (CT [0006]). Kashima et al also teaches a downtime was carried out for 24 seconds, which would be expected to reduce the remaining beam intensity to a range of 0.01 to 0.1 because applicant teaches stopping for 1 second reduced As beam intensity to about 1/14 and an As beam intensity within the claimed range after approximately 50 seconds

(See applicant's pg 9 of the specification and applicant's Fig 4). Furthermore, Kashima et al teaches a supply downtime t2 to reduce superfluous group V element deposition in a heterointerface (CT [0006]), which clearly suggests residual group V element concentration is a result effective variable. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Yokogawa et al and Kashima et al by optimizing the residual group V element to obtain the claimed range by conducting routine experimentation thereby obtaining a steep heterointerface. Also, the combination of Yokogawa et al and Kashima et al teaches arsine gas is efficiently exhausted in the growth vessel and is filled up with a phosphine gas instead (CT [0007]), thus the combination of Yokogawa et al and Kashima et al clearly suggest the arsine (first group V element) beam intensity should be reduced as low as possible, i.e. 0. A prima facie case of obviousness exists when the claimed range and the prior art range do not overlap but are close enough such that one skilled in the art would have expected them to produce products having the same properties. Titanium metal Corp. Am v Banner, 778 F.2d 775, 783, 227 USPQ 773, 779 (Fed. Cir. 1985).

Referring to claim 2, the combination of Yokogawa et al and Kashima et al teaches a first step of forming a IIIaVa thin film, a second step of suspending the supply of all the thin film raw materials, then supply of Vb is resumed first, which clearly suggests applicant's second step, and then supplying group IIIb for growth of an IIIbVb thin film, which clearly suggests applicant's third step of irradiating Group III elements in addition to continuously irradiating the molecular beam of the second group V element (CT [0005]-[0006])

Referring to claims 3 and 5, the combination of Yokogawa et al and Kashima et al teaches a first semiconductor layer of InGaAs and a second semiconductor layer of InP ('518 para [0008] and [0160]).

Response to Arguments

4. Applicant's arguments with respect to claim 1-3 and 5 have been considered but are moot in view of the new ground(s) of rejection.

5. Applicant's arguments filed 8/23/2010 have been fully considered but they are not persuasive.

Applicant's argument that the purpose of time periods t1 and t2 in Kashima is different from the objectives of the presently claimed invention is noted but not found persuasive. The fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). Kashima teaches a first step of supplying Va and IIIa molecular beams to form a first compound semiconductor layer; and discontinuing supply of all raw materials to efficiently exhaust gas in the growth vessel and then fill up with Vb and IIIb gases (CT [0005], [0006] and [0007]) to form steep hetero interfaces.

Applicant's argument that Kashima teaches time periods that ensure specific amount of the group Va element remains on the surface unlike the presently claimed invention which

reduces the reamining beam intensity is noted but not found persuasive. First, Kashima teaches the one molecular of As is from reevaporation of As, not from the molecular beam of As, which has already been closed during the down time (CT [0006]-[0007]). Second, Kashima teaches closing the shutters of the first semiconductor materials during t2, thus the molecular beam intensity is 0. In regards to the remaining beam intensity, the down time is carried out for 24 seconds and arsine is efficiently exhausted by filling up with phosphine gas, thus clearly suggests reducing any remaining arsine from the beam to zero.

Applicant's argument regarding unexpected results for the claimed range of 0.1 to 0.01 is noted but not found persuasive. First, applicant has not shown any comparsion with the closest prior to show unexpected results. Second, applicant alleges that reducing the beam to less 1/10 or less reduces the amount of As mixed to 0.05 or less, which is expected since reducing the amount of As would be expected to reduce the amount of As in the subsequent layers. Likewise, this effective is recognized in Kashima which teaches efficiently exhausting Arsine to control the deposition of superfluous Group V element in a heterointerface (CT[0006]-[0007]) by adjusting downtime. Third, applicant has not shown any criticality for the endpoint 1/100 the same result of reducing the As mixed amount would be expected for 0, i.e. the same result would be expected for less than 1/100. Fourth, the arguments are not commensurate with the scope of the claims as arguments are directed to specific materials and etchants etc, which the claims are not limited to any particular materials.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,206,969 teaches purging a MBE growth chamber (Abstract).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW SONG whose telephone number is (571)272-1468. The examiner can normally be reached on M-F 11:00-7:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Kornakov can be reached on 571-272-1303. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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